Notice of Allowability	Application No.	Applicant(s)	
	10/779,734	KUROKI, KOJI	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Pre-Exam Response (Jun 29, 2004) and Interviews (Mar 1-3, 2005)*.

2. ☒ The allowed claim(s) is/are *1-6 (now renumbered as 1-2, 5, 3-4, and 6, respectively for printing purposes)*.

3. ☒ The drawings filed on *18 February 2004* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 02182004
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *03032005* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to the applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with the applicant's representative Donald R. Studebaker (Reg. No. 32,815) on Mar 3, 2005.

The application has been amended as follows:

Claim 1, line 4: deleted "(A)";

line 6: changed "terminal" to --end--;

line 7: deleted "(A)";

line 15: deleted "(B)";

line 18: deleted "(B)";

line 27: deleted "(C)";

line 32: deleted "(C)";

line 35: deleted "(C)";

line 43: deleted "(B)"; added --, and an output of the first inverter circuit is coupled to the second node, and an output of the second inverter circuit is coupled to the first node-- after "signal";

Claim 2, line 3: changed "terminal" to --end--;

line 6: added --(N5)-- after "transistor";

Claim 3, line 4: deleted "(A)";

line 8: deleted "(B)";

line 13: deleted "(C)";

line 14: deleted "(B)";

line 18: deleted "(D)";

line 19: deleted "(A)";

line 20: changed "terminal" to --end--;

line 21: deleted "(C)";

line 22: deleted "(E)";

line 24: deleted "(D)";

line 25: deleted "(E)";

line 27: deleted "(E)";

line 34: deleted "(B)";

line 35: added --, and an output of the first inverter circuit is coupled to the first node, and an output of the second inverter circuit is coupled to the second node-- after "signal";

Claim 4, line 5: changed "non-cut out" to --non-cutout state--;

Claim 5, line 5: added --state-- after "non-cutout"; and

Claim 6, line 6: added --state-- after "non-cutout".

The majority of changes made to claims 1 and 3 removed the reference designators with respect to the various nodes identified within the claims. Although the applicant had originally requested all of the reference designators to be removed, it was determined that those related to

the transistors should be left in the claims to clearly distinguish one transistor from another (e.g. both inverter circuits comprise "a PMOS transistor" and "an NMOS transistor"), wherein the various nodes are easily identified by use of their respective ordinal number (e.g. "first", "second", etc). Since the connections of the inverter circuits' outputs to the first/second nodes were deemed critical by the examiner, both claims 1 and 3 were amended to clearly recite those relationships. The use of "terminal", with respect to the fuse mounting section, was changed to --end-- in claims 1 (line 6), 2 (line 3), and 3 (line 20) to provide consistent labeling throughout the claims. Also for consistency, line 6 of claim 2 had the second NMOS transistor identified by its corresponding reference designator, and claim 4 had "non-cut out" changed to correspond to "non-cutout" cited in both claims 5 and 6. Each of claims 4-6 had the term --state-- added to more clearly identify what the "non-cutout" referred to, otherwise the phrase "its non-cutout" could possibly be confusing.

The above changes were discussed over at least four telephone interviews occurring over three days (i.e. Mar 1st –3rd), wherein the final approval for the changes was given on Mar 3rd.

With the above changes, there is no known objection or rejection remaining within the present application.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

None of the prior art references reviewed and considered shows or discloses the fuse detection circuit as recited within independent claims 1 and 3. More specifically, none of the references clearly shows/discloses: 1) the same control signal being connected to the gate of each of the first-second PMOS transistors, as well as to the gate of each of the first-third NMOS

transistors as recited within claim 1 (upon which claims 2, and 4-5 depend); or 2) the first NMOS transistor as recited within claim 3 (upon which claim 6 depends), wherein this transistor is coupled between a fifth node and ground, and its gate is connected to the same control signal provided to the first/second PMOS transistors. Since there is no motivation to modify or combine any prior art reference(s) to ensure these specific limitations are met, the claims are deemed patentably distinct over the prior art of record.

Claims 1-6 are allowed, and have been renumbered as claims 1-2, 5, 3-4, and 6, respectively for printing purposes. The claims were renumbered to group related claims closer together with respect to their independent claim.

PRIOR ART

The prior art references on the accompanying PTO-892 are cited for interest and documentation purposes only. Although both references show and disclose circuitry that comprises the majority of elements (e.g. all but one of them) recited within the claims, there is no motivation to modify either of these references to ensure the fuse detection circuit reads on every limitation recited within either independent claim 1 or 3. For example, Fig. 19 of Hidaka shows a fuse detection circuit that closely corresponds to the applicant's own Fig. 1, which corresponds to the circuit recited within claim 1. However, Hidaka's first PMOS transistor 226, first NMOS transistor ATRp (within PBL), second PMOS transistor 228, second NMOS transistor ATRp (within /PBL), and third NMOS transistor 225 are controlled by their own respective control signal (e.g. /SA, SA, or /PRG), wherein claim 1 clearly recites that the gate of each of these five transistors is connected to the (same) "control signal". The reference of Lim et al. shows a circuit in Fig. 5 that closely corresponds to the applicant's own Fig. 3, which corresponds to the

circuit recited within claim 3. However, Lim's circuit lacks a first NMOS transistor coupled between a fifth node and ground as recited, wherein its gate would be connected to the same control signal that is also connected to the gates of the first and second PMOS transistors. For example, not only would Lim's circuit have to be modified to have an NMOS transistor coupled between the common connection node of 202,204 (i.e. fuse resistor elements) and ground, that transistor would also have to be controlled by control signal MRS1B connected to first/second PMOS transistors 214/206. Therefore, the claimed limitations read over these relevant prior art references.

The prior art references cited on the IDS submitted Feb 18, 2004 were reviewed and considered. Both references show/disclose a fuse detection circuit, but do not show or disclose at least the first and second inverter circuits as recited within each of independent claims 1 and 3.

Any comments considered necessary by the applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

3 March 2005